UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/417,980	10/13/1999	LINUS TORVALDS	TRANS12	8220

7590 07/22/2003

Wagner Murabito & Hao LLP
Two North Market Street
Third Floor
San Jose, CA 95113

EXAMINER
ELLIS, RICHARD L

ART UNIT	PAPER NUMBER
2183	4

DATE MAILED: 07/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n N .	Applicant(s)	
	09/417,980	TORVALDS ET AL.	
	Examin r	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-4 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,3 and 4 is/are rejected.

7)☒ Claim(s) 2 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. Claims 1-4 are presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

3. Claim 3 is rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A) The scope of meaning of the following terms are unclear:

1. "at which that state is known" claim 3 lines 18-19; It is unclear from the context of the claim which of multiple previously recited states the word "that" is referring to as being known. There is a claimed state at lines 5-6, 11-12, and 15-16 of the claim, any of which could be the state referenced by the word "that" at lines 18-19. As such, the claim is unclear and indefinite.

4. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a)shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 3-4 are rejected under 35 USC § 102(b) as being anticipated by Robinson et al., U.S. Patent 5,307,504.

Robinson et al. taught (e.g. see figs. 1-5b) the invention as claimed (as per claim 1), including a data processing ("DP") system comprising:

A) a method for use by a host microprocessor (col. 4 lines 40-44) which translates sequences of instructions (col. 2 lines 35-36) from a target instruction set for a target processor (col. 4 lines 38-40) to sequences of instructions for the host microprocessor

(col. 4 lines 35-38) comprising the steps of;

B) beginning execution of a first sequence of target instructions by committing state of the target processor and storing memory stores generated by previously-executed sequences of instructions at a point in the execution of instructions at which state of the target processor is known (col. 7 lines 22-38);

C) beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores (col. 7 lines 22-38, previous instructions state is committed before next instruction execution is begun);

D) attempting to execute the speculative sequence of host instructions until another point in the execution of target instructions at which state of the target processor is known (col. 7 lines 15-37, the system attempts to execute the "X instruction granule" to completion if possible);

E) rolling back to last committed state of the target processor and discarding memory stores generated by the speculative sequence of host instructions if execution fails (col. 7 lines 51-60), and

F) beginning execution of a next sequence of target instructions if execution succeeds (it is inherent within Robinson et al.'s system that if execution succeeds, it (the system) will proceed on to the next sequence of target instructions, because to do otherwise would result in the system not functioning for it's intended purpose).

7. As to claim 3, Robinson et al. taught a method of use by a host microprocessor which translates sequences of instructions from a target instruction set for a target processor to sequences of instructions for the host microprocessor comprising the steps of;

A) beginning execution of a first sequence of target instructions by committing state of the target processor and storing memory stores generated by previously-executed sequences of instructions at a point in the execution of instructions at which state of the target processor is known (col. 7 lines 22-38);

B) executing a sequence of host instructions from the first sequence of target instructions commencing immediately after committing state of the target processor and storing memory stores previously generated by a execution until another point in the translation of target instructions at which state of the target processor is known (col. 7 lines 15-37, the system will inherently repeat these steps for each X instruction granule);

C) beginning execution of a next sequence of target instructions by committing state of the target processor and storing memory stores generated by the execution of the first sequence of target instructions at a point in the execution of target instructions at which that state is known (col. 7 lines 25-37, each X granule commits it's state at a known point, namely the disclosed G3 and G4 groupings, and therefore has "stored memory stores" and "committ[ed] state" at a point "at which that state is known"), and;

D) executing a sequence of host instructions from the next sequence of target instructions commencing immediately after committing state of the target processor and storing memory stores generated by the execution of the first sequence of target instructions until another point in the execution of target instructions at which state of the target processor is known (col. 7 lines 15-37, because the system inherently repeats the disclosed steps for each X granule, it will perform the same steps for each "next sequence" of target instructions encountered.).

8. As to claim 4, Robinson et al. taught a method for use by a host microprocessor which translates sequences of instructions from a target instruction set for a target processor to sequences of instruction of the host microprocessor comprising the steps of;

A) translating a first speculative sequence of host instruction from the first sequence of target instructions (col. 6 line 30 to col. 7 line 51) from a point in the translation of target instructions at which state of the target processor is known (as detailed at col. 7 lines 21-37, the state of the target processor is known at each G3+G4 grouping of an X granule),

B) ending the first sequence of target instructions in response to encountering a branch from the first sequence in the target program by (although Robinson et al. does not disclose branches per. se., he does disclose that the X target instruction set is a VAX (TM) machine,

see col. 5 lines 61-64, and therefore, inherently contains branch instructions, which Robinson et al. must ultimately handle in order to achieve his intended purpose of translation compatibility, see col. 11 line 66 to col. 12 line 9);

C) branching to a branch sequence of target instructions (Robinson et al.'s code will inherently contain "branch target instructions" which implement the functionality of branches present within the target code),

D) committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions (col. 7 lines 21-37), and;

E) ending execution of the first sequence of target instructions if a branch is not taken from the first sequence by;

F) rolling back to last committed state of the target processor and discarding memory stores generated by the speculative sequence of host instructions if execution fails (col. 7 lines 38-60), and

G) committing state of the target processor and storing memory stores generated by the first sequence at the end of the sequence of target instructions at which state of the target processor is known (col. 7 lines 21-37).

9. Claims 1 and 3-4 are rejected under 35 USC 102(e) as being anticipated by Babaian et al., U.S. Pre-Grant Publication 2002/0,092,002 A1.

Babaian et al. taught (e.g. see figs. 1-5) the invention as claimed (as per claim 1), including a data processing ("DP") system comprising:

A) a method for use by a host microprocessor (fig. 1, 102) which translates (fig. 2, 202, 203) sequences of instructions from a target instruction set for a target processor (fig. 2, 116) to sequences of instructions for the host microprocessor ("Binary Translated Code) comprising the steps of;

B) beginning execution of a first sequence of target instructions by committing state of the target processor and storing memory stores generated by previously-executed sequences

of instructions at a point in the execution of instructions at which state of the target processor is known (para. 0032);

C) beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores (para. 0044 and 0063);

D) attempting to execute the speculative sequence of host instructions until another point in the execution of target instructions at which state of the target processor is known (para. 0048);

E) rolling back to last committed state of the target processor and discarding memory stores generated by the speculative sequence of host instructions if execution fails (para. 0070-0080), and

F) beginning execution of a next sequence of target instructions if execution succeeds (inherently, Babaian et al. will begin the next sequence if execution is successful, because to do otherwise would not result in any useful work from the system).

10. As to claim 3, Babaian et al. taught a method of use by a host microprocessor (fig. 1 102) which translates sequences of instructions (fig. 2, 202, 203) from a target instruction set (116) for a target processor ("Foreign Code and Data") to sequences of instructions for the host microprocessor ("Binary Translated Code") comprising the steps of;

A) beginning execution of a first sequence of target instructions by committing state of the target processor and storing memory stores generated by previously-executed sequences of instructions at a point in the execution of instructions at which state of the target processor is known (para. 0032);

B) executing a sequence of host instructions from the first sequence of target instructions commencing immediately after committing state of the target processor and storing memory stores previously generated by a execution until another point in the translation of target instructions at which state of the target processor is known (para. 0064-0068 and 0070, second recovery point is another "point ... at which state of the target processor is known");

C) beginning execution of a next sequence of target instructions by committing state of the target processor and storing memory stores generated by the execution of the first sequence of target instructions at a point in the execution of target instructions at which that state is known, and (para. 0064-0068 and 0070, third recovery point is another "point ... at which state of the target processor is known");

D) executing a sequence of host instructions from the next sequence of target instructions commencing immediately after committing state of the target processor and storing memory stores generated by the execution of the first sequence of target instructions until another point in the execution of target instructions at which state of the target processor is known (further translated code sequences within Babaian et al. will themselves inherently have additional recovery points as detailed at para. 0064, et seq.).

11. As to claim 4, Babaian et al. taught a method for use by a host microprocessor (fig. 1, 102) which translates sequences of instructions (fig. 2, 202, 203) from a target instruction set (116) for a target processor ("Foreign Code and Data") to sequences of instruction of the host microprocessor ("Binary Translated Code") comprising the steps of;

A) translating a first speculative sequence of host instruction from the first sequence of target instructions from a point tin the translation of target instructions at which state of the target processor is known (para. 0055-0057),

B) ending the first sequence of target instructions in response to encountering a branch from the first sequence in the target program by (para. 0055, "jnc");

C) branching to a branch sequence of target instructions (para. 0056, "JNC Label"),

D) committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions (para. 0042-0049), and;

E) ending execution of the first sequence of target instructions if a branch is not taken from the first sequence by;

F) rolling back to last committed state of the target processor and discarding memory

stores generated by the speculative sequence of host instructions if execution fails (para. 0073-0080), and

G) committing state of the target processor and storing memory stores generated by the first sequence at the end of the sequence of target instructions at which state of the target processor is known (para. 0038-0048).

12. Claims 1 and 3-4 are rejected under 35 USC 102(e) as being clearly anticipated by Kelly et al., U.S. Patent 5,958,061.

As to claims 1 and 3-4, Kelly et al. clearly taught the claimed invention, see for example col. 9 lines 25-40, col. 12 line 34 to col. 13 line 65, col. 16 line 7 to col. 18 line 38 including all the claimed steps of storing state, holding memory stores, and rolling back to a stored state upon the occurrence of failure of execution.

13. Claim 2 is objected to as being dependent upon a rejected base claim, but would render the base claim allowable if bodily incorporated into the base claim such that the new base claim included all of the original limitations of the base claim, any intervening claims, and the objected claim.

14. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

15. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone numbers for this Group are: After-final: (703) 746-7238; Official: (703) 746-7239; Non-Official/Draft: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
July 17, 2003

RICHARD L. ELLIS
PRIMARY EXAMINER